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Single-Step Formation of ZnO/$ZnWO_x$ Bilayer Structure via Interfacial Engineering for High Performance and Low Energy Consumption Resistive Memory with Controllable High Resistance States

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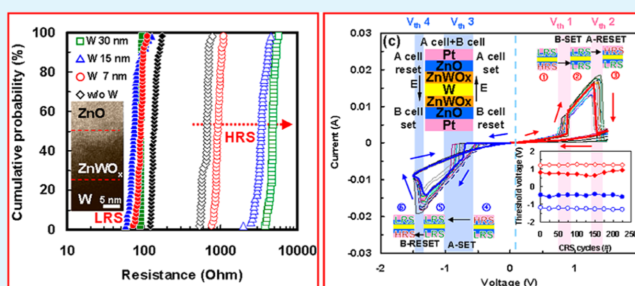
Supporting Information

ABSTRACT: A spontaneously formed ZnO/$ZnWO_x$ bilayer resistive memory via an interfacial engineering by one-step sputtering process with controllable high resistance states was demonstrated. The detailed formation mechanism and microstructure of the $ZnWO_x$ layer was explored by X-ray photoemission spectroscopy (XPS) and transmission electron microscope in detail. The reduced trapping depths from 0.46 to 0.29 eV were found after formation of $ZnWO_x$ layer, resulting in an asymmetric $I-V$ behavior. In particular, the reduction of compliance current significantly reduces the switching current to reach the stable operation of device, enabling less energy consumption. Furthermore, we demonstrated an excellent performance of the complementary resistive switching (CRS) based on the ZnO/$ZnWO_x$ bilayer structure with DC endurance >200 cycles for a possible application in three-dimensional multilayer stacking.



KEYWORDS: *resistive switching memory, $ZnWO_x$ interface engineering, ZnO, complementary resistive switching (CRS), sneak path*

1. INTRODUCTION

Development of resistive random access memory (ReRAM) is one of mainstreams for next generation nonvolatile memories (NVM) because of its fast switching speed, low power consumption, excellent endurance, and easy integration with current devices.[1−5] A two terminal stacking configuration is generally considered as the best structure to reach a highly stacking density of ReRAM devices via three-dimensional (3D) crossbar process, which can geometrically achieve highest packing density with a maximum stacking size of $4F^2$ (F = minimum feature size).[6] Sneak path, an inherent disadvantage, is typically resulted from the current flowing through the neighboring devices while employing two terminals stacking together for the 3D crossbar application. To avoid the sneak path, a connection with other passive devices, such as rectifying diode (1D1R), switching transistor (1T1R), and threshold selector (1S1R) as the switching elements is a simple way to prevent the whole system from the influence of the bypass current as the device is operated at a low resistive state, whereas the incorporation of passive devices would make fabrication process much complicated.[7−12]

A demonstration of connecting two bipolar ReRAM cells using solid electrolytes as switching materials has been reported to solve the sneak paths, but the overall processes are relatively complicated.[2,13] Therefore, the material choice with a simple fabrication process is an important consideration. Metal oxides, such as HfO_2,[4] WO_3,[14] TiO_2,[15] ZnO,[16,17] and NiO,[18] are promising materials for ReRAM applications because of their controllable compositions with an easy sputtering process at low temperature. Among these metal oxide materials, zinc oxide (ZnO) has many superior characteristics in optics and electronics, such as a wide and direct band gap of ∼3.37 eV, adjustable electrical properties via the doping of different dopants, and much lower synthetic temperature.[19] ZnO-based thin film ReRAM devices were found to have a promising resistive switching behavior with either unipolar or bipolar resistive switching characteristics. a The preferred c-axis orientation of the ZnO film enables a high power consumption due to high reset current of 20−40 mA and leakage current along grain boundaries, which results in unstable operation and is a challenge in developing the ZnO-based RRAM.[16,17] Some literature reported that the increase in the resistance in high resistance state could be achieved by controlling dopants, such as Ni and Li.[20,21] Formation of interfacial metal oxide on resistive switching metal oxide layer, namely bilayer structure, after capping a reactive metal as electrode can usually act as the oxygen reservoir, providing sufficient oxygen vacancies to improve switching uniformity and reliability. However, a simple

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and direct way of single-step formation of bilayer structure in order to reduce to fabrication process and process cost is essential.[4]

In this regard, we demonstrated a spontaneous formation of $ZnO/ZnWO_x$ bilayer structure via interface engineering by one-step sputtering process for the ReRAM application. The advantages of the spontaneously formed $ZnWO_x$ layer beneath the ZnO layer can increase the high resistance value of devices but also reduce the compliance current of maintaining a stable operation of devices, enabling less power consumption. The detailed formation mechanism of $ZnWO_x$ layer during the sputtering process was explored by X-ray photoemission spectroscopy (XPS) measurements. Furthermore, the complementary resistive switching (CRS) based on the $ZnO/ZnWO_x$ bilayer structure via antiserial stacking to avoid the sneak path was demonstrated with DC endurance >200 cycles for a possible application in three-dimensional multilayer stacking.

2. EXPERIMENTAL SECTION

Fabrication of Devices. RF-magnetron sputtering system was used to prepare Pt/ZnO/Pt and $Pt/ZnO/ZnWO_x/W$ devices. The bottom W/Pt electrode was deposited with W thickness of 7, 15, and 30 nm on the $Ti/SiO_2/Si$ (100) substrate. Subsequently, 30 nm thick ZnO film was deposited upon the W layer at room temperature with a power density of 2 W/cm^2 and a working pressure of 5×10^{-3} Torr, respectively. During sputtering process, the $ZnWO_x$ layer could be formed simultaneously. Pt top electrodes were patterned on ZnO films by a shadow mask with the diameter of 200, 100, and 50 μm.

Characterization. Keithley 4200 semiconductor parameter analyzer under DC sweeping mode was used to measure $I-V$ characteristics of devices. During voltage sweeping mode, the positive bias was defined as the current flowed from Pt top to W bottom electrode grounded. The nanostructure of the $Pt/ZnO/ZnWO_x/W$ was examined by field-emission transmission electron microscopy (FE-TEM, JEM-3000F, JEOL operated at 300 kV with point-to-point resolution of 0.17 nm) and atomic composition was analyzed by electron dispersive spectrometer (EDS). Meanwhile, the depth profile and the interfacial bonding state of different stacks were examined by X-ray photoelectron spectroscopy, which were calibrated by Pt bottom electrode (XPS, Perkin-Elmer Phi 1600 ESCA system, operated at 25 mA/15 kV). The etching rate, beam current density, and accelerating voltage of argon plasma were 0.12 nm/s (3.5 nm in 30 s), and 2.8×10^3 A/m^2 (25 mA in 9 mm^2), and 15 keV, respectively.

3. RESULTS AND DISCUSSION

A ZnO film as a resistive switching layer switched by top platinum (Pt) and bottom tungsten (W) metal layers as the contact electrodes was prepared by a sputtering process. A very thin layer, namely, $ZnWO_x$ layer could be simultaneously formed as a mediated layer under the ZnO layer while the sputtering ZnO layer was being formed on the W electrode layer. The $Pt/ZnO/ZnWO_x/W$ bilayer structure is schematically illustrated in inset of Figure 1(a, where the different thicknesses of W layers on Pt electrodes from 7 to 30 nm were prepared. The corresponding current-to-voltage ($I-V$) switching loops for the $ZnO/ZnWO_x$ bilayer and a pure ZnO layer were measured for comparison as shown in Figure 1a, respectively. Basically, "SET" process is defined as a sudden increasing of current owing to a switching of the resistive state from high resistance state (HRS) to low resistance state (LRS) after a SET bias was applied with compliance current of 10 mA while "RESET" process, which is opposite to the "SET" process, exhibits a sudden decreasing of current due to the resistance switching from the LRS to the HRS after a RESET bias was applied. The switching mechanism is called bipolar

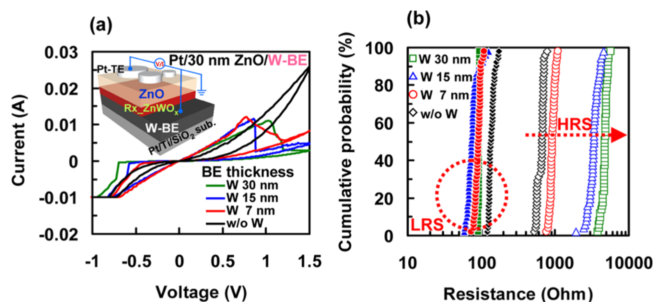

Figure 1. (a) Typical $I-V$ behaviors of with and without formation of $ZnO/ZnWO_x$ bilayer structures with different as-grown W layer thicknesses. Inset shows the configuration of devices. (b) Cumulative probabilities of LRS and HRS for Pt/ZnO/Pt and $Pt/ZnO/ZnWO_x/$ Pt devices with different as-grown W layer thicknesses.

switching. For all devices at the HRS, the slopes of $I-V$ curves were distinctly found to be decreased with increasing of as-grown W layer thicknesses, revealing the increasing of device resistance owing to the increasing of the $ZnWO_x$ layer thickness formed from the as-grown W layer after sputtering process of ZnO layer (Figure 1a). Figure 1b shows the cumulative probability as the function of resistance with different thicknesses of as-grown W layers from 7 to 30 nm with read voltage of 0.1 V, respectively. The HRS increases with the increasing of as-grown W layer thicknesses, resulting in the enhanced HRS/LRS ratio of up to ~300%, whereas saturation could be obtained as the thickness of the as-grown W layer over ~15 nm.

To confirm the phase and structure of $ZnWO_x$ layer, grazing incidence X-ray diffraction (GIXRD) was used to analyze crystal structure of layers by changing different incident angles from 0.3 ° to 0.5°, for which the structure information from top ZnO to bottom $ZnWO_x$ layers can be found (see Figure S1 in the Supporting Information). The (002) peak in ZnO layer can be clearly indexed at the incident angle of 0.3°, whereas a very slight shift at (002) peak to low angle can be found at the higher incident angle >0.4° because of the increase in lattice constant. The results confirm that the formation of the $ZnWO_x$ layer is resulted from either the substitutional sites of Zn atoms replaced by W atoms or interstitial sites of ZnO lattice occupied by W atoms in tetrahedral or octahedral sites. In addition, the $ZnO/ZnWO_x$ bilayer structure, a cross-sectional transmission electron microscope (TEM) image is imperative to unveil the detailed microstructures as shown in Figure 2(a) with the as-grown W layer thickness of 30 nm. A different contrast observed in the TEM image represents a stacking sequence of $ZnO/ZnWO_x/W$ layers, for which the $ZnWO_x$ layer with a thickness of ~15 nm could be found (see Figure S2a in the Supporting Information). The corresponding high resolution TEM image obviously provides clear interfaces of ZnO/ $ZnWO_x$ and $ZnWO_x/W$, with which lattice spacings of 0.26 and 0.29 nm can be identified, corresponding to ZnO (002) and $ZnWO_x$ (011) planes, respectively (see Figure S2b in the Supporting Information). Furthermore, the atomic concentrations from electron dispersive spectrometer (EDS) analyses at each layer as marked as positions A–D in Figure 2a are shown in Table 1 with a beam size of ~0.5 nm controlled by the STEM mode, confirming the spontaneous formation of the $ZnWO_x$ layer with atomic concentrations of ~46 at % Zn, 25 at % O, and ~29 at % W, respectively. To further confirm the formation of the $ZnWO_x$ layer, we show the corresponding

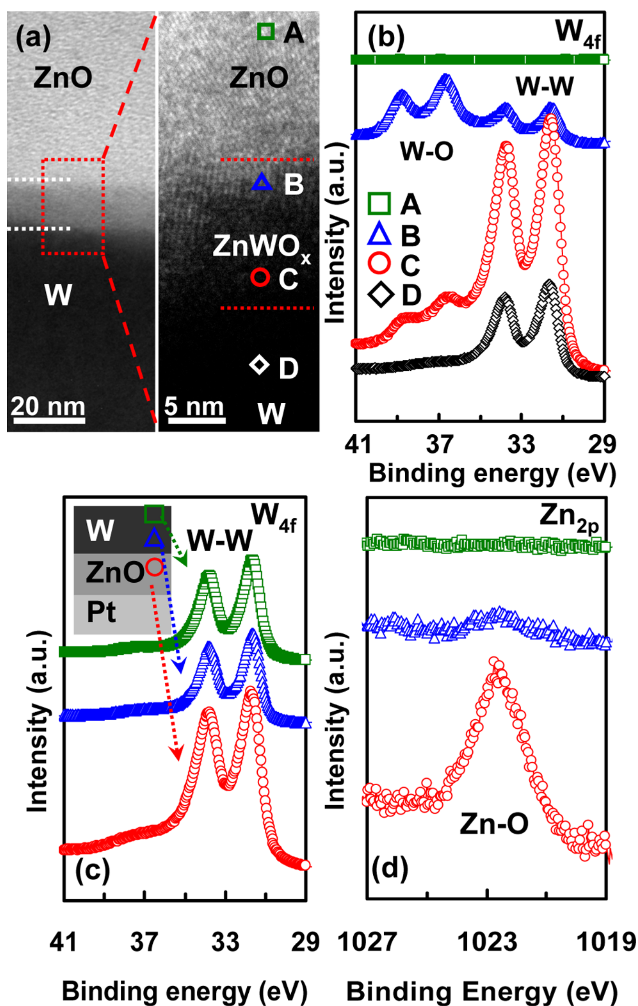

Figure 2. (a) Cross-section TEM images of Pt/ZnO/$ZnWO_x$ (15 nm)/W device. Right-hand side shows the corresponding HRTEM image. (b) XPS spectra of W 4f-edge taken from different positions. (c, d) XPS spectra for W/ZnO/Pt device at W 4f-and Zn 2p-edges, respectively. Inset in (c) shows the configuration of W/ZnO/Pt device.

Table 1. EDS Quantitative Results at Positions from A to D

positions	Zn (at %)	O (at %)	W (at %)
A	59	41	0
B	46	25	29
C	42	29	32
D	<1	8	91

XPS results of W 4f-edges at different positions (A–D) in Figures 2b at different points related to TEM image (Figure 2a and Figure S3a in the Supporting Information).[22] No W signal can be found in position A, indicating the pure formation of ZnO film without any contamination of W layer during the sputtering process. In position B, peaks at 31.5 and 33.5 are associated with tungsten oxide, corresponding to $4f_{7/2}$ and $4f_{5/2}$ edges, whereas peaks at 36.5 and 38.8 eV are resulted from tungsten metal ($4f_{7/2}$ and $4f_{5/2}$ edges), providing an obvious evidence of the simultaneously formed $ZnWO_x$ layer at the interface of ZnO and the W layers.[22] Noting that the intensities of $4f_{7/2}$ and $4f_{5/2}$ edges gradually decrease from the interface of ZnO/$ZnWO_x$ (position B) to the W layer, indicating no formation of $ZnWO_x$ layer, which is also consistent with the XPS results at Zn 2p-edge (see Figure S3b in the Supporting Information).[22] From Ellingham diagram, the direct formation of WO_x layer is impossible because the Gibbs free energy of ZnO (approximately −650 KJ/mol) is lower than that of WO_3 (approximately −500 KJ/mol) at 300 K. Therefore, we believed that the formation of $ZnWO_x$ results from reaction of the W layer with active O^{2-} ions during the ZnO sputtering process, thereby effectively lowing the absolute Gibbs free energy of WO_x.[1,23,24]

To prove our assumption, we prepared an opposite sputtering process, namely, W (∼80 nm)/ZnO (∼30 nm)/Pt for comparison. The corresponding XPS spectra of W 4f and Zn 2p edges from the W to the ZnO layers for the W/ZnO/Pt structure are shown in panels c and d in Figure 2, respectively (see Figure S4 in the Supporting Information for more XPS spectra of the W/ZnO/Pt structure). Inset in Figure 2c) indicates the estimated positions for each XPS spectrum, concluding that no direct formation of the $ZnWO_x$ layer at the interface of the W/ZnO layers can occur. The results also prove that the introduction of active O^{2-} ions during the ZnO sputtering process is most likely a main reason for the spontaneous formation of the $ZnWO_x$ mixed layer, whereas the saturated HRS/LRS ratio could result from the saturated resistance at the HRS once the thickness of the spontaneously formed $ZnWO_x$ layer reaches a saturated thickness, which is ∼53 nm in our case. (A HRTEM image of the $ZnWO_x$ layer with W thickness of 7 nm is shown in Figure S2c in the Supporting Information.)

The ZnO layer provides resistance change due to the rupture/recovery of filament paths in the ZnO layer controlled by applied bias (see Figure S5 in the Supporting Information for more detailed switching mechanisms),[15,25] whereas the $ZnWO_x$ layer acts not only as the base layer to increase the resistance of the device at the HRS but also as the reservoir for the supplement of oxygen ions, enabling a stable and recognizable performance as shown in Figure 3a with a logarithmic plot at the fixed W thicknesses of 15 and 30 nm. Usually, the compliance current has to be applied over a critical value to tune the device from the HRS into the LRS, enabling an adequate R_{OFF}/R_{NO} ratio and longer endurance.[26] For the Pt/ZnO/Pt devices without the $ZnWO_x$ layer, the compliance current of ∼10 mA was necessary to apply to achieve the stable endurance of ∼100 cycles, although the compliance current could be reduced after the formation of the $ZnWO_x$ layer to maintain the identical endurance operation as shown in Figure 3b, for which the smallest compliance currents of 5 and 1 mA were demanded to operate the devices with as-grown W layers of 15 and 30 nm at an electrode diameter of 200 μm, respectively. The reduced compliance current refers to the less energy consumption so that the low RESET current ($I_{RESET,\ max}$) could be achieved with the increase in the as-grown W layer thicknesses as shown in Figure 3b. Furthermore, the maximum power consumption with and without $ZnWO_x$ layers was also calculated by $V_{RESET}I_{max}$ as shown in Figure 3b. Notably, the operation power of ∼0.67 mW could be achieved after the formation of the $ZnWO_x$ layer with the as-grown W layer of 30 nm at electrode diameter of 200 μm. However, the power consumption can be further reduced with a decrease in electrode diameter. To further demonstrate the reduced power consumption, we measured $I-V$ behaviors with different diameters from 200 to 50 μm for the devices with as-grown W layers of 30 nm as shown in Figures 3c. The corresponding compliance current and power consumption were shown in

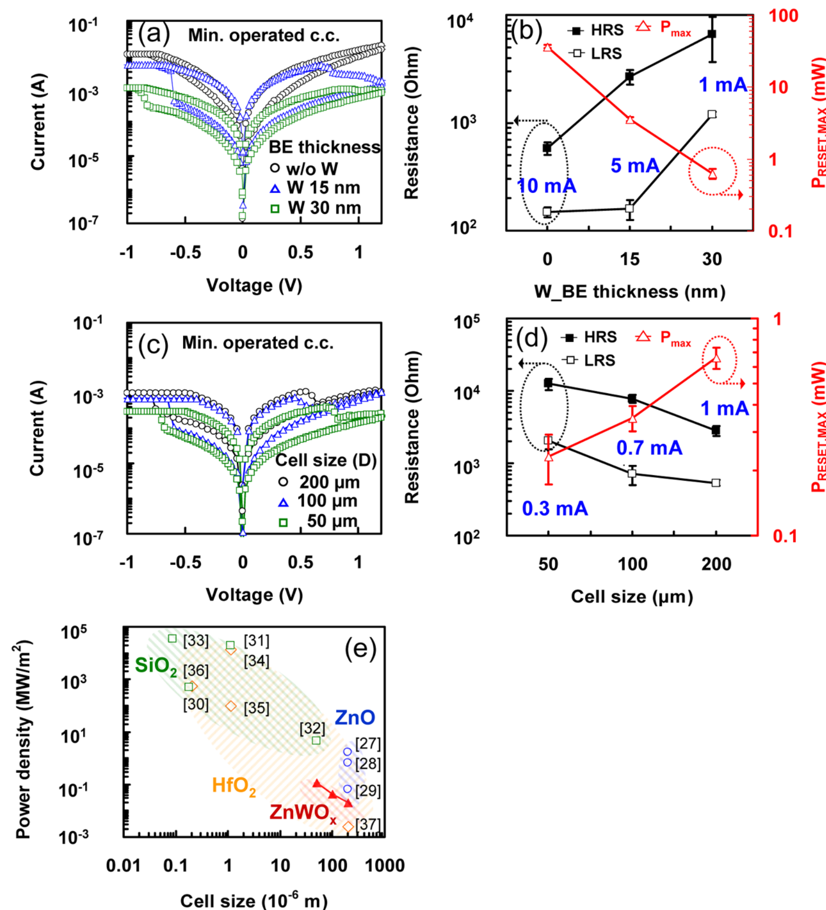

Figure 3. (a) Logarithmic plots of $I-V$ behaviors for devices with and without formation of $ZnO/ZnWO_x$ bilayer structure. Noting that as-grown W layers were increased from 15 to 30 nm. (b) The smallest compliance current for a stable device switching and the lowest power consumption without and with the formation of the $ZnWO_x$ layer. (c) Logarithmic plots of $I-V$ behaviors for devices with and without formation of $ZnO/ZnWO_x$ bilayer structure at different electrode diameters from 200 to 50 μm, respectively. (d) The smallest compliance current for a stable device switching and the lowest power consumption without and with the formation of the $ZnWO_x$ layer at different electrode diameters from 200 to 50 μm. (e) Power densities at different MIM systems with different electrode diameters.

Figure 3d, for which the smallest compliance currents of 0.7 and 0.3 mA were measured with electrode diameters of 100 and 50 μm, respectively (see Figure S7 in the Supporting Information for detailed $I-V$ behaviors). As a result, the power consumption can be further reduced into 0.23 mW at the electrode diameter of 50 μm, yielding a power density of ~1.2 × 10^{-1} MW/m^2. In order to convince the low consumption after the formation of the $ZnWO_x$ layer, the power density from the different MIM systems, e.g., M/ZnO/M,[27−29] M/SiO_2/M,[30−33] and M/HfO_2/M,[34−37] where M was defined as varied electrodes and were extracted as shown in Figure 3e. The detailed $I-V$ behaviors and the corresponding power densities at different electrode diameters were shown in Table S2 in the Supporting Information. Consequently, the device after the formation of the $ZnWO_x$ layer indeed exhibits the lowest power consumption than other ZnO RRAM and is comparable with HfO_2 system, demonstrating a reduced operation power through the self-formed bilayer metal oxide structure via one-step sputtering process.

To shed light on how the $ZnWO_x$ layer influences the conducting mechanism of ZnO film, the characteristic curves of Pt/ZnO/$ZnWO_x$ (~15 nm)/W and Pt/ZnO/Pt devices were measured for comparison. In general, Schottky emission, Poole−Frenkel emission, and space-charge limited current (SCLC) transports were the typical transport mechanisms at the HRS, which indicates different kinds of traps/barriers at the interface or in the bulk of oxide layers.[16,17,38] By plotting ln (J/E) as the function of $E^{1/2}$ as shown in Figure 4a, the conducting mechanism, which involves hopping of electrons via trapped states excited by an electrical field, could be expressed as follows[16,17,38]

$$\ln\frac{J}{E} = \sqrt{E}\left(\frac{q}{rkT}\sqrt{\frac{q}{\pi\varepsilon_0\varepsilon_r}}\right) + \ln(q\mu N_t) - \frac{q\psi_t}{KT}$$

where the q, μ, N_t, k, T, ψ_t, ε_o, and ε_r are charge of an electron, mobility of hopping trap, density of trap, Boltzmann's constant, temperature, depth of trap, free space permittivity, and dynamic dielectric constant, respectively. Note that r is a coefficient ranging between 1 and 2 related to an electron compensation effect among trapping sites.[38−40] A pure Poole−Frenkel transport happens as r = 1, indicating a few defects inside the dielectric layer, whereas a larger number of defects formed in the interface of metal and dielectric layer eventually result in the modified Poole−Frenkel transport, namely Schottky-like emission as r = 2.[38,41] By using ZnO refractive index (n) of ~2.2,[42,43] the $r \approx 1.0$ could be extracted by fitting a linear slope from the ln (J/E) versus $\sqrt{E}$ of the Pt/ZnO/Pt device (Figure 4a). However, the $r \approx 1.7$, namely the Schottky-like emission, plays an important role in the Pt/ZnO/$ZnWO_x$ (15 m)/W

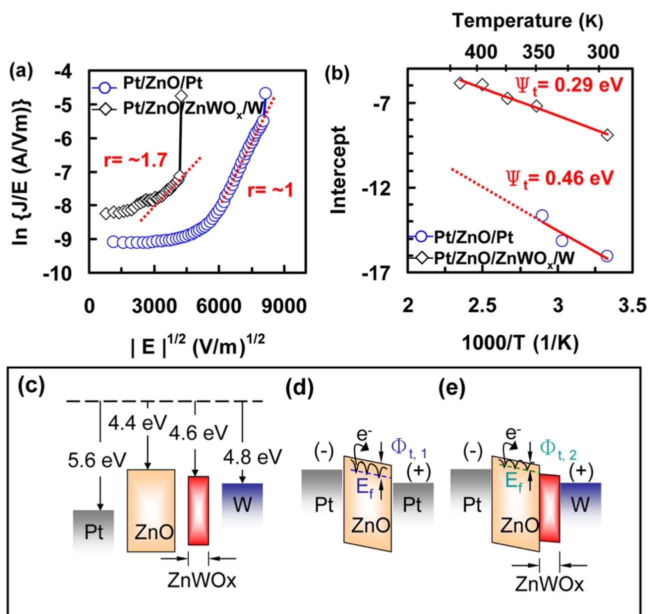

Figure 4. (a) Plotting of ln (J/E) as the function of $E^{1/2}$ for Pt/ZnO/Pt and Pt/ZnO/$ZnWO_x$ (15 nm)/W devices. (b) The intercepts of Pt/ZnO/Pt and Pt/ZnO/$ZnWO_x$ (15 nm)/W devices as the function $1/T$. (c) Schematic band diagram of each layer. (d, e) Band alignment after negative bias contact was on Pt electrode for two devices, namely Pt/ZnO/Pt and Pt/ZnO/$ZnWO_x$/Pt, where $\Phi_{t,1}$ and $\Phi_{t,2}$ represent trap depth.

device. Furthermore, the trap depth (ψ_t) of ~0.46 eV for the Pt/ZnO/Pt device at the HRS could be extrapolated from an intercept of ln(J/E) as the function of temperatures as shown in Figure 4b, namely, an Arrhenius plot, which is consistent with the value reported in the literature.[21] However, the ψ_t could be reduced into ~0.29 eV after the formation of the $ZnWO_x$-based layer, which enhances opportunities of electron hopping as showed in Figure 4b, thereby significantly reducing the SET current and leading to an asymmetric I−V behavior.[44] It also explains why negative and positive polarities for SET and RESET processes are exclusively demanded to operate the Pt/ZnO/$ZnWO_x$/W device because the $ZnWO_x$ layer beneath the ZnO layer can effectively create an Ohmic-like contact for carriers injected easily from bottom electrode into the device (see Figure S8 in the Supporting Information).[14,45] To shed light the formation of the Ohmic-like contact, we plotted the schematic band diagrams for Pt/ZnO/Pt and Pt/ZnO/$ZnWO_x$/W devices as shown in Figures 4c, for which work functions of 5.6 and 4.8 eV for Pt and W with electronic affinities of 4.4 and 4.6 eV for ZnO and $ZnWO_x$ layers were used for band alignment.[14,48,49] A barrier can be found in ZnO/Pt interface as shown in Figure 4d. However, the barrier can be further reduced after the formation of the $ZnWO_x$ layer, resulting in the formation of the Ohmic-like contact and the lower trap depth ($\Phi_{t,1} > \Phi_{t,2}$) as shown in Figure 4e.

In addition, in metal−ferroelectric−semiconductor (MFS) heterostructure such as $BaTiO_3$(BTO)/ZnO, the interface polarization coupling between ZnO and oxide can lead to asymmetry $I-V$ behaviors, which influences the HRS and LRS.[46,47] As a result, the reversible resistive switching between a high-resistance state (HRS) and a low-resistance state (LRS) is resulted from different charge carriers accumulated or depleted at the interface of ferroelectric−semiconductor by dipolar electric field, where the ferroelectric layer provides a hysteresis loop to influence the interface polarization coupling on the surface of semiconductor layer.[46,47] However, no obviously hysteresis characteristics were found in $I-V$ behaviors of Pt/ZnO/$ZnWO_x$/W and Pt/ZnO/Pt RRAM devices (see Figure S9 in the Supporting Information), indicting that the influence of interface polarization coupling on interface polarization coupling on the resistance states of the ZnO/$ZnWO_x$ bilayer is a minor issue, for which the limited V_{max} of 1.5 V was applied because of the occurrence of resistance switching for Pt/ZnO/$ZnWO_x$/W RRAM device around −2 V. As a result, the ZnO layer provides the resistance change because of the rupture/recovery of filament paths controlled by applied bias, whereas the $ZnWO_x$ layer acts an interface layer to enhance opportunities of electron hopping to the electrode and the ZnWOx layer acts an interface layer to influence the $I-V$ behavior.

The complementary resistive switching (CRS) memory has been proposed to avoid the sneak path for a 3D cross-point configuration application by utilizing two the bipolar resistive memories connected back to back without any switching elements.[4,50] To demonstrate the CRS concept based on our ZnO/$ZnWO_x$ bilayer memristor, we connected the ZnO/$ZnWO_x$ (A cell) and the inverse $ZnWO_x$/ZnO (B cell) bilayer memristor in parallel in order to simplify the fabrication process of CRS device. Noting that the thickness of the $ZnWO_x$ layer for A and B cells is ~15 nm (30 nm thick W layer case). The corresponding asymmetric and inversely asymmetric $I-V$ behaviors for A and B cells are shown in panels a and b in Figure 5, with which the cell configuration and directions of

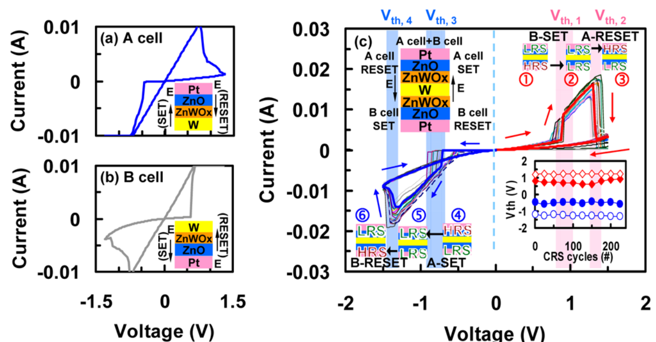

Figure 5. (a) $I-V$ behaviors of cell A (Pt/ZnO/$ZnWO_x$/W) and (b) cell B (W/$ZnWO_x$/ZnO/Pt). Inset show the corresponding device configuration. (c) I−V sweeps of the ZnO/$ZnWO_x$/W/$ZnWO_x$/ZnO CRS device. Inset shows the device configuration and the corresponding resistive switching for two cells. All the thickness of $ZnWO_x$ layer is ~15 nm.

applied electrical fields after SET/REET processes were illustrated in insets of panels a and b in Figure 5, respectively. Figure 5c shows the corresponding $I-V$ sweeps of the Pt/ZnO/$ZnWO_x$/W/$ZnWO_x$/ZnO/Pt (A cell+ B cell) CRS device, which are superimposed $I-V$ behaviors by two bipolar memristor (see the Supporting Information, Figure S10 for detailed operation). Inset shows the direction of applied electric field and device configuration during SET and RESET processes. Obviously, tour distinct biases, V_{th1} to V_{th4}, enable us to define the CRS device with four different states, namely, "ON" state as both cells are in the LRS, "1" state as A cell is in the HRS and B cell is in the LRS, and "0" state as A cell is in the LRS and B cell is in the HRS.[4,46] Noting that the "OFF" state appears only in an initial state as both A and B cells are in the

HRS. In addition, different resistance values of "1" and "0" states are contributed to deviation of electrode size patterned by shadow mask owing to different resistance deviation between A and B devices. In addition, a hysteresis loop due to accumulated charges resulting from capacitance of MIM configuration during continuous DC scan may be another reason to slightly change resistance difference at different bias sweep. The CRS device can be very stably operated with an endurance of >200 cycles because of the spontaneous formation of the $ZnWO_x$ interlayer, indicating that the CRS based on the $ZnO/ZnWO_x$ bilayer structure has highly possible promising as three-dimensional multilayer stacking. Furthermore, the controllable resistance in HRS by the interface engineering because of the formation of the $ZnWO_x$ layer could be further applied in different fabrication processes and materials to improve electrical properties of RRAM devices.

4. CONCLUSIONS

In summary, we have demonstrated a spontaneously formed $ZnO/ZnWO_x$ bilayer structure by one-step sputtering process via interface engineering with controllable HRS from $\sim 1 \times 10^3$ to $\sim 1 \times 10^4$ Ω for resistive memory. The detailed formation mechanism and microstructure of the $ZnWO_x$ layer was explored during the sputtering process by XPS and TEM. For the Pt/ZnO/Pt devices without $ZnWO_x$ layer, the compliance current was necessary to be applied at 10 mA to achieve the stable endurance of ~100 cycles while after the formation of $ZnWO_x$ layer, the smallest compliance currents of 0.3 mA was measured at the electrode diameter of 50 μm, yielding the reduced power consumption of ~0.23 mW with the power density of $\sim 1.2 \times 10^{-1}$ MW/m^2. The asymmetric *I*–*V* behavior and negative/positive polarities for SET/RESET processes are explained by the reduced trapping depths after formation of $ZnWO_x$ layer. In particular, the reduction of compliance current significantly enables less energy consumption. Furthermore, the CRS based on the $ZnO/ZnWO_x$ bilayer structure was demonstrated, exhibiting an excellent performance for practical applications of 3D multilayer stacking memory devices.

■ ASSOCIATED CONTENT

Supporting Information

XRD spectra; TEM and HRTEM images of the Pt/ZnO/$ZnWO_x$ (15 nm)/W device; XPS spectra of the Pt/ZnO/$ZnWO_x$/W and W/ZnO/Pt devices; switching mechanism of ZnWOx layer as the reservoir; Resistance ratios of HRS/LRS at different device sizes; *I*–*V* behaviors of the Pt/ZnO/$ZnWO_x$/W devices with different compliance currents at different electrode diameters; A logarithmic plot of the corresponding ln(I) versus ln(V) with the Pt/ZnO/Pt and Pt/ZnO/ZnWOx/W devices; *I*–*V* behaviors of Pt/ZnO/ZnWOx/W and Pt/ZnO/Pt RRAM devices; Processes of operating the CRS device; Table S1 for the minimum operating current compliance with different top electrode sizes; Table S2 for comparison of the power consumption with different metal oxide memristors. These materials are available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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